

Date: 29th October 2024

To,

I-Stem
Govt. of India

From,

Sandeep P Agnihotri
#15, B-006, Oasis Nine,
7th Cross, 1st Main,
ISRO Layout,
Bengaluru 560078

Sub: Please consider my I-Stem registration without academic identification.

Honoured Sir, or Madam,

I, Sandeep P. Agnihotri, am writing to inform you that I am currently unemployed. I have roughly 17 years of research and academic experience, with twelve years in academics.

I will be required to access the COMSOL Multiphysics FEM tool as part of the ongoing IEEE Sensor Council and ISSS MPW Run training for which I have enrolled.

As previously mentioned, I might not be able to register on the I-Stem site without providing proof of my academic ID.

I respectfully ask that you view my situation as unique and permit me to use the tool during the training.

You have my gratitude, and I will thank you in all my future endeavours.

Regards and thanks,
Sandeep P. Agnihotri.

Sandeep P. Agnihotri

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📍 No. 15, B - 006, Oasis Nine, 7th Cross, 1st Main, ISRO Layout, 560 078, Bengaluru, India (Home)

🚩 Indian

About Me

I am an experienced professional with a strong foundation in electronics and communication, complemented by a background in teaching and mentoring engineering students. My early career involved hands-on research in semiconductor processing and device characterization, which I conducted in renowned international laboratories. Over the past decade, my focus shifted primarily to academia, with limited recent research activity. I am eager to transition into the corporate sector, leveraging my technical knowledge and problem-solving skills to contribute effectively, while embracing new learning opportunities in a dynamic environment.

Education

07/2004 – 10/2006 Noida, India	Master of Technology (Nanotechnology) Amity University Uttar Pradesh
09/1999 – 06/2003 Bengaluru, India	Bachelor of Engineering (Electronics and Communication Engineering) VTU, Belagavi (APS College of Engineering, Bengaluru)

Professional Experience

03/2013 – 09/2023 Mumbai, India	Assistant Professor SVKM's NMIMS Mukesh Patel School of Technology Management and Engineering • Delivered courses in electronics and communication, including Analog Circuits, Digital Electronics, and Wireless Communication, focusing on real-world applications to enhance student learning and industry readiness. • Provided mentorship and academic guidance to students, encouraging practical problem-solving skills and technical competence, preparing them for careers in engineering and technology. • Supervised Master of Technology projects with an emphasis on applying advanced engineering principles to solve real-world challenges, aligning academic work with industry standards. • Led the coordination of NBA accreditation processes, managing Self-Assessment Report preparations, and demonstrating strong organizational and project management skills. • Organized and facilitated technical workshops on CMOS, Mixed Signal, and RF VLSI Design in collaboration with IIT Kharagpur, bridging the gap between academia and industry by exposing students to current technological advancements.
03/2012 – 02/2013 Hyderabad, India	Assistant Professor Nizam's Institute of Engineering and Technology • Taught the course on Antenna and Wave Propagation, providing students with a strong foundation in communication engineering concepts and practical applications. • Supported student learning through one-on-one mentorship and guidance, helping them develop technical skills and confidence in their coursework.

03/2008 – 03/2011
Grenoble, France

Research Engineer

Fondation Nanoscience

- Conducted growth of II-VI semiconductor heterostructures using Molecular Beam Epitaxy (MBE), contributing to the development of advanced materials with practical applications.
- Performed device fabrication in a cleanroom environment, utilizing top-down nanofabrication techniques, including lithography and etching, to create precise semiconductor structures.
- Executed detailed characterization of materials and devices using Scanning Electron Microscopy (SEM) and low-temperature electrical transport measurements, ensuring accuracy and quality in research outputs.
- Collaborated with cross-functional teams to troubleshoot and optimize processes, enhancing efficiency and reliability in semiconductor device development.
- Applied technical problem-solving skills to address complex challenges in semiconductor processing, demonstrating a proactive approach to research and development tasks.

01/2007 – 10/2007
Bengaluru, India

Project Assistant

Department of Instrumentation, IISc

- Assisted in the deposition of rare earth metal oxides on silicon substrates using Pulse DC, RF, and Ion Beam techniques, supporting the development of high-k gate oxide materials.
- Conducted capacitance-voltage measurements on MOS capacitors, contributing to research in advanced semiconductor materials and device performance analysis.
- Collaborated with senior scientists to execute experimental protocols, gaining valuable insights into semiconductor research methodologies and industry standards.

Skills

Research Skills

- **Semiconductor Processing:** Molecular Beam Epitaxy, Nanofabrication, Lithography, Etching.
- **Characterization Techniques:** Scanning Electron Microscopy (SEM), Profilometry, Electrical Transport Measurement.
- **Aquainted with working in Class - 1000 cleanroom environment.**

Organizational Skills

- **Stakeholder interaction and Communication Skills:** Student interaction, student facilitator in achieving learning objectives.
- **Accreditation Expertise:** NBA Accreditation Coordination, SAR Preparation, Workshop Coordination.
- **Adptability and willingness to learn.**

Publications

Analyzing Two Stage CMOS LNA for Wireless Interconnect

- P Mahajan, S P Agnihotri, "Analyzing Two Stage CMOS LNA for Wireless Interconnect", 2019 IEEE 5th International Conference for Convergence in Technology (I2CT) Proceedings, DOI: 10.1109/I2CT45611.2019

Conferences and Seminars

08/2009

St. Petersburg, Russia

14th International Conference on II-VI Compounds

- *Oral Presentation on "Fabrication of II-VI semiconductor sub-micron pillars"*

06/2009

Krynica - Zdroj, Poland

38th International School & Conference on the Physics of Semiconductors, "Jaszowiec" 2009

- *Poster Presentation on "Fabrication of II-VI based submicron pillars: an approach for single quantum dot confinement"*