

Indian Science Technology and Engineering facilities Map (I-STEM)

Invites application for

Partial financial support for creating skilled manpower (Format-4)

Format for requesting support for accessing and using facilities through the I-STEM web portal.

(i) Profile:

- a. Name of the Training Coordinator: **Dr. Shipra Upadhyay**
- b. Name of the R&D facility:
VLSI Lab — Training on System-on-Chip (SoC) Design Flow and verification
- c. Name of the Department: **Electronics and Communication Engineering**
- d. Name of the Institution: **Atria Institute of Technology, Bangalore**
- e. Mob. No.8004959188
- f. Email ID: **shipra.u@atria.edu**

Details of training

Name of R&D Equipment: **Vivado ML Enterprise Edition, FPGA SoC Development Boards**

Duration and Hours of Usage of Tools/day (Practical Training/tutorials): **3 hours/Day (5 Days)**

Duration of Theoretical Training: **3hours/ Day (5 Days)**

No. of trainer Involved: **Five**

*External Trainers: **Two***

*Institute (internal) Trainers: **Three***

Instructors (Internal): **Five**

No. of Manpower to be trained per training (Duplication and overlapping of candidate may be avoided): **Twenty**

Details of the Training module/Course Content		
Module -1	Lecture -1 (3 hrs)	ASIC Flow: Introduction to Verilog language constructs, RTL coding, RTL integration, Connectivity checks, Functional Verification, Synthesis & STA, Gate level simulations, Power aware simulations
	Lab -1 (3 hrs)	Lab session on RTL coding, simulations and verification
Module -2	Lecture -2 (3 hrs)	SOC Architecture overview, SOC design concepts, SOC verification concepts, SOC Components.
	Tutorial -1 (3 hrs)	Assignments and Quiz on SOC Test bench architecture and SOC verification concepts

Module -3	Lecture -3 (3 hrs)	FPGA Architecture: Internals of FPGA, Logic implementation, FPGA Architectures of various FPGA vendors, Anti-fuse and SRAMS, Logic elements and Look-up Tables, Dedicated multipliers, Distributed RAM, Shift registers, Kintex, Zynq, Virtex Architectures
	Tutorial -2 (3 hrs)	Assignments and Discussions
Module -4	Lecture -4 (3 hrs)	Introduction and usage of IP cores, Design constraining and pin locking Timing analysis, slack calculation, Data loss due to large skew, Maximum skew calculations Period constraint, Area and Power Constraints, Static Timing Analysis
	Lab -2 (3 hrs)	Lab session on FPGA Implementation using IP cores, Timing analysis, slack calculation, Area and Power Constraints, Static Timing Analysis
Module -5	Lecture -5 (3 hrs)	FPGA programming, Translate, Map, Floor plan, Place and Route, Post map and Post P&R simulation, XDC constraints, Reading and analysing reports-post synthesis, Post map simulation, Post P&R simulation, Configuring FPGAs, FSM Extraction
	Lab -3 (3 hrs)	Lab session on FPGA prototyping

No. of Training in a Year: 1

Details of the Budget (in):

Training Cost:

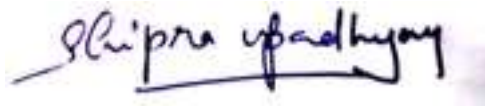
S. No.	Type	Cost in hours (30 Hours)			Total cost (₹)
1	Training cost	Trainer	Training Hours	Total (₹)	58500/-
		External Trainer 1 @5000 ₹/hr	2	10000	
		External Trainer 2 @5000 ₹/hr	3	15000	
		3 Internal Trainers (Atria Institute of Technology) @2000 ₹/hr for each	10	20000	
		5 Lab Instructors (Atria Institute of Technology) @1500 ₹/hr for each	9	13500	
2	Training materials support	100,000			100,000/-
3	Sum	--			1,58500/-

Lodging Cost: NIL

Study Materials Cost: 50,000 ₹

(Please submit the details of the budget required. The Institution must be required to submit the original bills (Consolidated) signed by the Head of the Institution and Finance Controller for the reimbursement.)

Note: Proposed proposal must be executed within stipulated duration (max. 12 month) to avoid fund availability issues. Travel form will be provided by the I-STEM office. The users will submit the technical report, original invoice (duly signed by the Head of the Institution) raised by the Host Institution through I-STEM portal only along with a copy of the travel forms and original tickets through post to the Nodal Officer, I-STEM, Indian Institute of Science, Bangalore. A scan copy of all the documents may be sent in advance.

A handwritten signature in blue ink, reading "Sriprata Upadhyay", with a horizontal line underneath the name.